EVALUATION OF CRYOGENIC READOUT ELECTRONICS FOR ASTRO-F

Toyoki Watabe[1], Takanori Hirao[1], Hiroshi Shibai[1],Mitsunobu Kawada[1], Hirohisa Nagata[1], Yasunori Hibi[1], Manabu Noda[2], Takahiro Nakagawa[3]

[1]Nagoya University, Furo-cho Chikusa-ku Nagoya 464-8602 Japan
[2]Nagoya City Science Museum, 17-1 Sakae 2-chome Naka-ku Nagoya 460-0008 Japan
[3]The Institute of Space and Astronautical Science Yoshinodai, Sagamihara, Kanagawa 229-8510

ABSTRACT

We have developed low-noise, low-power Cryogenic Readout Electronics (CRE) for the far-infrared detectors which have been fabricated for Far Infrared Surveyor (FIS) on board ASTRO-F, the first Japanese infrared astronomical satellite. The CRE will be mounted beside the detector unit and operated at cryogenic temperature as low as ~1.8K. The detector was built with a Capacitive Trans-Impedance Amplifier (CTIA) for FIS. In addition to low noise and low power, high amplifier gain is needed for the CTIA. Through three iteration cycles, we have trial manufactured and evaluated the differential amplifier and CTIA at cryogenic temperature (4.2K). We established the open-loop voltage gain of the differential amplifier to be over 300 and power consumption to be less than 10μW.

INTRODUCTION

ASTRO-F has two focal plane instruments, the far infrared Surveyor (FIS) and the Infrared Camera (IRC). FIS has two detector arrays, the SW for short wave (50~120μm) and the LW for long wave (100~200μm). Both arrays, LW and SW, employ gallium doped germanium (Ge:Ga) photoconductors which will be cooled to ~2K. Mechanical stress is applied to Ge:Ga for the LW detector array (Doi et al. 2001). The LW array has 100 (20x5) pixels and the SW array has 75 (15x5) pixels. Since the responsivity of Ge:Ga is strongly dependent on the bias voltage (V_b), it is essential to use a Capacitive Transimpedance Amplifier (CTIA) for the readout electronics. The advantage of the CTIA is that it compensates the bias voltage itself. The disadvantage of the CTIA is that it needs an inverting amplifier with large open-loop gain , like an op-amp. An integration capacitor and a reset switch (transistor) must be added to the amplifier. The requirements for the CRE of FIS are listed below:

- 2K operation
- Noise level : 1 $\mu V(Hz)^{-1/2}$ at 1Hz
- Power consumption 10 μW/channel
- open-loop gain > 1000

Contact information for T.Watabe: Email: watabe@u.phys.nagoya-u.ac.jp , phone (81) 52 789-5247

DESIGN

MOSFET

Fig.1 shows the schematic view of the MOSFET structure we have developed. 0.5 µm BiCMOS-process was baselined. An ion implantation doped contact channel was a special modification for this FET and it was essential for the improvement of the current-voltage characteristic at 4.2K.

Amplifier

Fig 2. shows the circuit diagram of the cryogenic differential amplifier. This amplifier has two inputs, an inverting input and a non-inverting input and optimum voltage for V1 and V2 are +1.8V and –1.8V respectively. We used this circuit for evaluation with no feedback to measure the open-loop gain like in an op-amp.

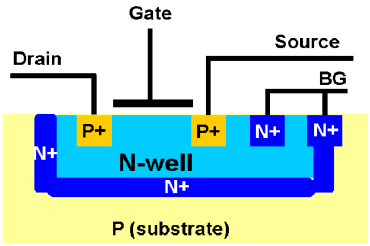

Fig 1. Model image of the cryogenic p-MOSFET. BiCMOS technology can make N^+ buried layer and ion implantation doped well contact was made.

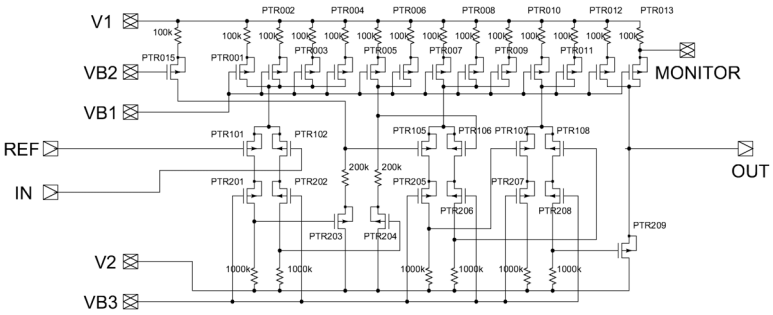

Fig 2. Circuit diagram of the differential amplifier. REF is the non-inverting input and IN is the inverting input.

CTIA

Fig.3 shows the block diagram of the CTIA with the test circuit. The CTIA is made of a high gain differential amplifier, an integration capacitor and a reset switch. For the integrating capacitor, the capacitance is fixed to 10pF for LW and 7pF for SW to optimize the signal to noise performance.

PERFORMANCE MEASURMENTS

MOSFET

We measured the characteristics at liquid helium temperature to extract the SPICE parameters for circuit simulation, to evaluate the noise performance, and to optimize the gate size of the MOSFETs. Fig 4 shows the I-V characteristics at 4.2K. The N-channel MOSFETs showed kink behavior in this voltage range, but the P-channel MOSFETs have no such anomalies at 1 µW power consumption at cryogenic temperature. We observed the short channel effect for the other MOSFETs at 4.2K and we rejected them.

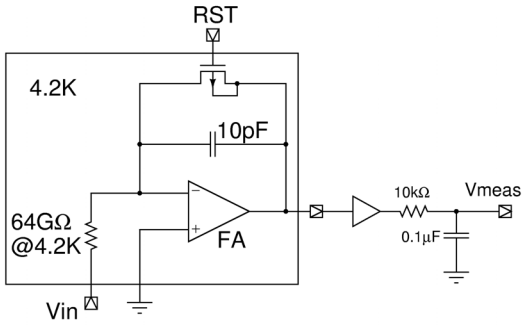

Fig 3. CTIA is in the square line.

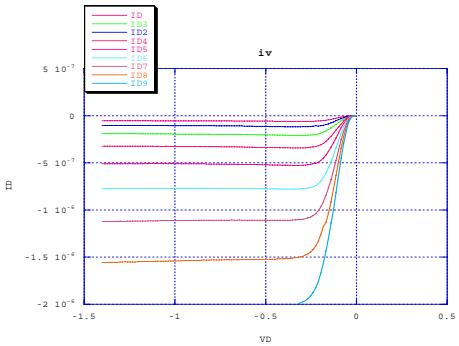

Fig 4. Drain voltage – drain current curves were measured at 4.2K. No kink behavior was observed; improvements of BiCMOS make good performance.

Cryogenic Amplifier

Fig 5 shows the test circuit and Fig 6 and 7 are measurement data. The performance of the cryogenic amplifier was measured as a non-inverting amplifier with feedback at 4.2K. The voltage gain can be calculated from equation (1). We did the conversion from amplifier gain to open-loop gain with the combination of R1 and R2. In this case, R1 was 1MΩ and R2 was 100kΩ.
"A" represents the open-loop gain of the cryogenic amplifier.

Closed-loop gain $G = 1 / (1 / A + R2 / (R1 + R2))\ Vsig$ (1)
Open-loop gain $A = Vout / (Vsig - R2 / ((R1 + R2)\ Vout)$

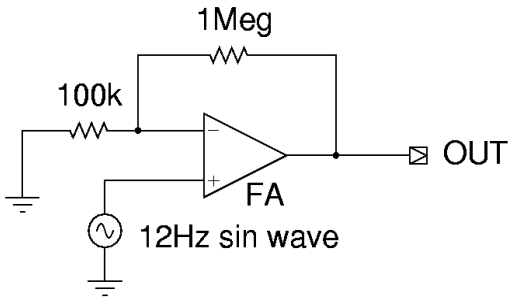

Fig 5. The test circuit for the cryogenic amplifier, FA.
The amplifier was cooled to 4.2K
Feed-back resister was not in the cryostat.

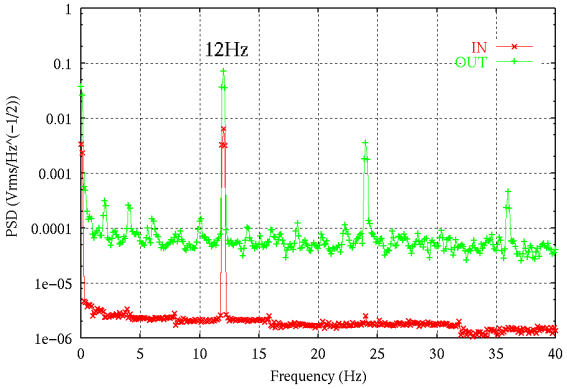

Fig 6. The power spectrum density of the input and output signal. The lower line corresponds to the input signal

CTIA

Figure 3 shows the test circuit with the CTIA block diagram. Fig 7 and 8 show the measured data for the CTIA. All test data were obtained at 4.2K. Figure 7 shows the test results obtained with a large open-loop gain amplifier, but figure 8 shows the results using a low gain amplifier.

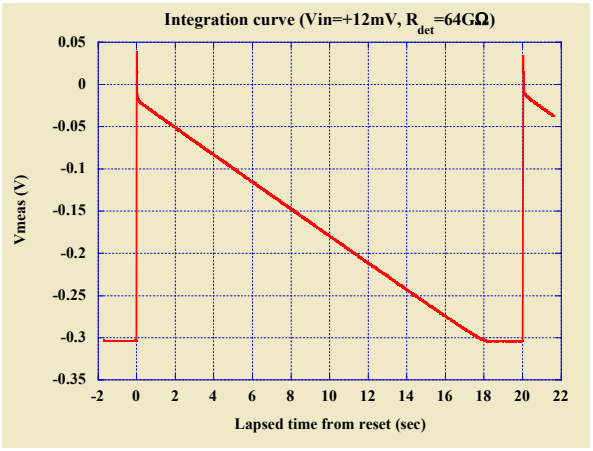

Fig 7. CTIA output signal at 4.2K
Dummy resistor was 64GΩ

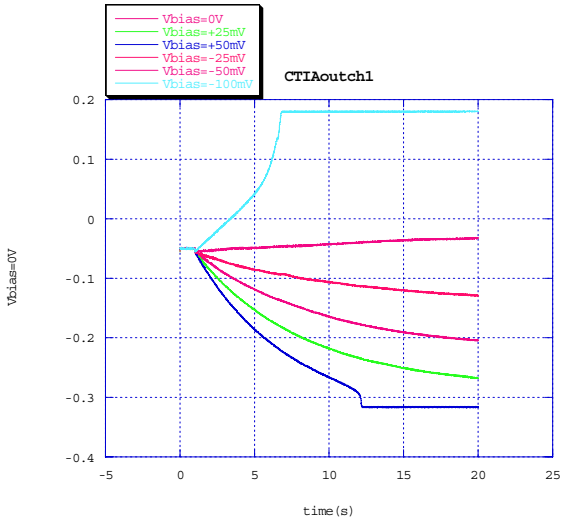

Fig 8. CTIA output signal at 4.2K
Dummy resistor was $1x10^{11}$ Ω

RESULTS

We have been testing the MOSFETs, cryogenic amplifier and CTIA circuit at the cryogenic temperature. MOSFETs were fabricated using the 0.5 μm improved BiCMOS process. The gate size of the MOSFETs is W/L = 20.6 μm/5 μm . We observed kink behavior for the n-channel MOSFETs, but we didn't observe kinks with the p-channel MOSFETs in the operation range, with a power consumption of ~1μW.
For the cryogenic amplifiers we observed an open loop gain of ~300, at a power consumption of less than 10μW and a noise level of ~3 μ $V(Hz)^{-1/2}$ at 1Hz.
We observed an integration curve for the CTIA with dummy resistors. We calculated the open-loop gain for the data shown in Fig 7 and Fig 8 and found ~100 and 5~10, respectively. The power consumption is within our requirement but more tests are needed for optimization and for further improvements. Small numbers of chips show good performance but other chips show poor gain and small output dynamic range.

ACKNOWLEDGEMENTS

We acknowledge Mr Kamoto, Mr Kimura, Mr Inabe and other staff at NTT Electronics Technology Corp. for their work and support. We are gratefull to all the members of the ASTRO-F team.

REFERENCES

1. Dierickx, B., Simoen, E.,Vermeiren, J.,Cos, S.,Claeye, C. et al., Optimization of CMOS Technology and Design for deep cryogenic analog Circuit, ESA Electronic Component Conference, ESA SP-313, 43, 1991
2. Doi, Y., Hirooka, S., Sato, A., Kawada, M., Shibai, H. et al., Large-format and compact stressed Ge:Ga Array for the ASTRO-F (IRIS) Mission, Advances in Space Resarch, 2001, in press
3. Glidden, R. M., Lizotte, S.C., Cable, J. S., Mason, L.W. and Cao, C.,Optimization of Cryogenic CMOS Processes for Sub-10K Applications, Proc. of SPIE, Vol. 1684, 2, 1992
4. Hiromoto, N., Fujiwara, M., Shibai, H., Hirao, T., Nakagawa,T. et al., Ge:Ga far-infrared Photoconductor 2D direct hybrid Array, Proc. of SPIE, Vol. 3354, 48, 1998
5. Noda, M., Shibai, H., Watabe, T., Hirao, T., Yoda, H., et al., Evaluation of Charge integrating Amplifiers with Silicon MOSFETs for cryogenic Readout, Proc. of SPIE, Vol. 3354, 247, 1998
6. Shibai, H., ASTRO-F: The Infrared Imaging Surveyor (IRIS) Mission, Advances in Space Resarch, 2001.,in press
7. Takahashi H., Shibai, H., Kawada, M., Hirao, T., Watabe, T., et al., FIS: far-infrared surveyor on board ASTRO-F (IRIS), Proc. of SPIE, Vol. 4013, 47, 2000.
8. Young, E. T., Davis, J. T., Thompson, C. L., Rieke, G. H., Rivlis, G., et al., Far-infrared imaging array for SIRTF, Proc. of SPIE, Vol. 3354, 57, 1998
9. Hirao, T., Hibi, Y., Kawada, M., Nagata, H., Shibai, H., Watabe, T., Noda, M. and Nakagawa, T., Cryogenic Readout Electronics with Silicon p-MOSFETs for the infrared astronomical Satellite ASTRO-F, Advances in Space Resarch, 2001, in press